# MMU Development

This sub-project relates to the design and implementation of a Memory-Management Unit to replace the existing hardware-based MMU in the uCOM.

1. The project can be realised in two steps. The first is to set up the MMU HDL and have it monitor commands to the existing MMU and shadow it’s output. It can return values to the host as well, so the host can see exactly which banks are mapped to which Areas without having to keep tabs using variables, which are often inaccurate. It can also be verified via SignalTap that it is outputting the correct values to the EA bus when this feature is added.
2. The second step will be to remove the hardware MMU and have the HDL MMU take over full control of the memory management function.

Results

1. It took about an hour whilst also doing my day job to get this step 80% completed. The FPGA keeps track of all interactions with the MMU now and returns the current value when the host reads the appropriate MMU IO port. This is a huge step forward in functionality for the uCOM and fixes the bug in the BANK command where Area 0 was never accurate, unless it had been manually changed.

I haven’t gone as far as implementing EA address bus control for the FPGA yet. There is no real pressure to make this extra feature or progress to Step 2, as the existing setup now provides all the functionality of the final setup. The only real benefits to progressing further would be the removal of the hardware MMU components, and the ability to possibly change the area/bank size, but this will mean an address bus change which requires a hardware modification to the entire PCB stack.